Handshake Rev A: Hardware Architecture

A PCB business card with a passive NFC tag. Tap it with a phone and it opens jamescronin.dev

Document	HSK-HW-001
Revision	Rev A as built, draft 4
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Date	8 November 2026
Status	Rev A complete. Five cards built by JLCPCB and delivered 6 Nov 2026; each one opens the site on an iPhone at about 4–5 cm. Resonance was not measured. Section 11 lists what was not done
Companion files	`HSK-PLAN-001_Project_Plan.md` (scope, budget, risks)

1. Purpose

Handshake is a business card made as a printed circuit board. It carries one NFC tag chip and a copper coil antenna around the edge of the card. There is no battery: a phone's NFC field powers the chip during a tap, and the chip answers with a web address, `jamescronin.dev/projects/handshake`. This document describes the Rev A board as built: what is on it, how it connects, and why each choice was made. Per-card links and a visit counter were planned but not built.

2. Requirements

ID	Requirement	How Rev A meets it	Result
R1	Any recent iPhone or Android phone opens the card's link with one tap, no app	NFC Forum Type 2 tag (ISO/IEC 14443A) holding one NDEF URI record; background tag reading on iOS and Android opens it in the browser	Met on iPhone. Android not tested
R2	Reads reliably at about 1–3 cm	Large 4-turn coil at the card edge, tuned to resonate slightly above 13.56 MHz, with an optional tuning capacitor (section 5)	Met: about 4–5 cm on all five cards
R3	Each card has its own link	Planned: a card ID in the URL, written when the card is programmed	Not built: all five cards hold the same link
R4	Casual rewrites of the link are blocked	32-bit write password on the tag after programming. It is sent unencrypted over NFC, so it deters casual overwrites but is not real security	Not met yet: no password set
R5	Wallet-sized and wallet-safe	ISO/IEC 7810 ID-1 outline, 85.6 × 54 mm, 3.18 mm corner radius, 0.8 mm board; parts on one side only	Met
R6	JLCPCB builds it complete, no hand soldering	One assembled part (C710403, Extended, in stock); single-side assembly	Met
R7	Looks deliberate	Black solder mask, ENIG finish, white silkscreen artwork on the back (JC mark and jamescronin.dev)	Met

3. Block diagram

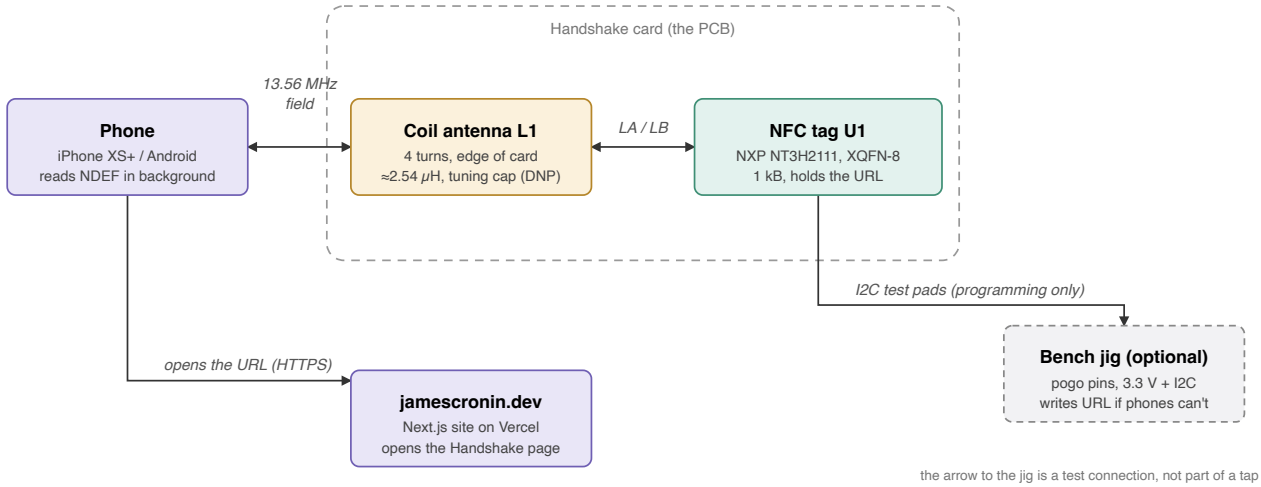


Figure 1. Rev A block diagram. Amber: antenna. Green: the one chip. Purple: phone and web side. The card has no power source; everything on it runs from the phone's field for the length of a tap.

4. Blocks

4.1 NFC tag chip

NXP NT3H2111W0FHKH (NTAG I2C plus, 1 kB), XQFN-8, 1.6 × 1.6 mm; JLCPCB C710403, Extended part, 48,206 in stock at $0.56 on 27 Oct 2026. It is an NFC Forum Type 2 tag (ISO/IEC 14443A) with an I2C port meant for a host microcontroller. Handshake has no host, so only the two antenna pins are used during a tap; the chip runs entirely from the phone's field. The I2C port stays reachable on bare pads so a bench jig can write the tag if phone apps cannot format it. The datasheet marks the package's centre pad "not for soldering". Backup if stock runs out: the SO-8 version NT3H2111W0FT1X (C2654859).

4.2 Antenna

A planar copper coil around the edge of the card, resonating with the chip's own input capacitance (section 5). No separate antenna part.

4.3 Web side

All five cards hold one link, `jamescronin.dev/projects/handshake`. The planned `/h/NN` route and per-card visit counter were not built, so the site cannot tell the cards apart.

5. Antenna

5.1 Target

The coil and the chip's input capacitance C_i form a parallel resonant circuit. The datasheet (Rev. 3.6, section 13.1) gives C_i = 44 / 50 / 56 pF (min / typ / max) between LA and LB at 13.56 MHz.

$$f_0 = 1 / (2\pi \sqrt{(L \cdot C)}) \quad \Rightarrow \quad L = 1 / (4\pi^2 \cdot (13.56\ \text{MHz})^2 \cdot 50\ \text{pF}) \approx 2.76\ \mu\text{H}$$

The design aims slightly below 2.76 μH so that the bare resonance lands a little above 13.56 MHz. Board and trace capacitance lower it, and the tuning capacitor can only lower it further. A tag that starts too low cannot be fixed without cutting copper.

5.2 Coil geometry

Calculated with the rectangular planar coil formula from NXP AN11276 (35 μm copper, exponent 1.8 for PCB coils). At full card size the inductance rises fast with turns, so 4 turns is right; the project plan's earlier "5–6 turns" would resonate around 9–11 MHz.

Outer coil	Track / gap	Turns	L	f_0 at C_i 44 / 50 / 56 pF
83.6 × 52.0 mm (1 mm inset)	**0.8 / 0.4 mm**	**4**	**2.56 μH**	**15.0 / 14.1 / 13.3 MHz**
82.6 × 51.0 mm (1.5 mm inset)	0.5 / 0.5 mm	4	2.82 μH	14.3 / 13.4 / 12.7 MHz
83.6 × 52.0 mm	0.8 / 0.4 mm	5	3.74 μH	12.4 / 11.7 / 11.0 MHz
83.6 × 52.0 mm	0.8 / 0.4 mm	3	1.56 μH	19.2 / 18.0 / 17.0 MHz

Rev A uses the first row's turns, track and gap. Wide 0.8 mm tracks keep the coil's resistance low (a higher Q gives more range). The formula is good to about ±10%. The planned second calculator check (ST eDesignSuite) and per-card resonance measurement were not done (section 11), so L and f_0 in this document are calculated and simulated values, not measurements.

5.2.1 As built

The coil footprint is generated by `tools/make_coil.py`, which builds the spiral, checks it against the design rules and refuses to write a footprint that breaks them. The as-built coil is set 0.2 mm further in than the first row above:

Outer coil (copper edge)	Edge to copper	Track / gap	Turns	L	f_0 at C_i 44 / 50 / 56 pF
83.2 × 51.6 mm	**1.2 mm** (1.6 mm to the outer centreline)	**0.8 / 0.4 mm**	**4**	**2.54 μH**	**15.05 / 14.12 / 13.34 MHz**

Why it moved. The card has rounded 3.18 mm corners and the coil has square ones, so the coil's corners come closer to the board edge than its straight sides do. At a 1 mm inset they came within 0.26 mm of the edge, under JLCPCB's 0.3 mm copper-to-edge minimum, where the router cutting the outline can nick the copper. At 1.2 mm the closest point is 0.55 mm. Inductance drops by under 1% (2.56 to 2.54 μH) and the resonance is unchanged at 14.1 MHz. The turns are evenly spaced, with a 0.40 mm gap everywhere; the spiral steps in one pitch per turn on the right-hand side, so both ends finish in the bottom-right corner next to the chip.

5.2.2 Simulation

The card was simulated in KiCad's ngspice as a parallel RLC circuit across LA–LB: coil 2.56 μH, chip input capacitance 50 pF, and the chip's power draw modelled as 5 kΩ (an estimate; NXP doesn't publish it). An AC sweep from 10 to 20 MHz with a 1 A test current puts the peak at 14.1 MHz (14.07 MHz by hand), with –3 dB points at 13.7 and 14.4 MHz, a

Q of about 20. At 13.56 MHz the model gives about half the voltage of the peak, which is the intended margin: board capacitance and the phone's coil both pull the resonance down. The project is in `Simulation/Handshake_Sim`.

5.3 Tuning capacitor

An optional capacitor across the antenna pins (C1, 0402), not fitted on any Rev A card. C0G only (stable with temperature). If a card measures above about 14 MHz, fit it to bring the resonance down:

$$C_{tune} = 1 / (4\pi^2 f_{target}^2 L) - C_{measured}$$

For example, with the as-built L = 2.54 μH and the target 13.56 MHz, the total needed is about 54.2 pF; a card measuring 50 pF in total takes about 4 pF (3.9 pF, the nearest E12 value).

6. Physical constraints

Item	Choice
Outline	ISO/IEC 7810 ID-1: 85.6 × 54 mm, 3.18 mm corner radius
Stack-up	2 layers, FR-4, 0.8 mm, 1 oz copper (thin enough for a wallet, stiff enough to feel like a board)
Finish	Black solder mask, ENIG (gold) on exposed copper, white silkscreen
Assembly	JLCPCB, top side only, one part; tuning capacitor not fitted
Quantity	Rev A: 5 cards

7. Tag data and security

- One NDEF URI record, prefix code 0x04 (`https://`) plus `jamescronin.dev/projects/handshake`, well inside the 888-byte user memory.
- **Blank chips:** the NT3H2111 ships with the Capability Container (page 3) set to all zeros (datasheet 8.3.10), so phone apps report the tag as unsupported or not NDEF. Each card was initialised once from an iPhone, using raw commands in NFC Tools: `A2:04:03:00:FE:00` (empty NDEF message), then `A2:03:E1:10:6D:00` (the Capability Container). Both replied `0A` (ACK). A normal NFC Tools write then stored the URL. The I2C pads were not needed.
- **Write protection:** not set. Any NFC app can currently overwrite or lock a card. Before handing cards out, set the 32-bit write password (PWD) and the AUTH0 page so writes need the password. Reading stays open, which phones need.
- **Limit:** a fixed URL can be copied, and a tag cannot prove it was tapped. A per-tap signature needs the NTAG 424 DNA, which JLCPCB cannot assemble today (plan, section 7).

8. Bring-up results

#	Test	Pass	Result, 6 Nov 2026
1	Chip orientation	Chip responds to a phone	**Pass, 5 of 5**
2	Resonance with a NanoVNA and a pickup loop, each card	13.56–14.5 MHz bare	**Not done**
3	Read with an iPhone (background reading)	URL opens	**Pass, 5 of 5**
4	Read with an Android phone	URL opens	**Not tested**
5	Read range	At least 1 cm	**Pass: about 4–5 cm on iPhone**

6	Write protection	A write without the password fails	**Not done: no password set**
7	Per-card route on the site	`/h/NN` counts once per visit	**Not built**

9. Key design decisions

Decision	Reason
NT3H2111, not NTAG 213/215/216	The NTAG 21x chips are sold as wafer or inlay, not in a package JLCPCB places; the NT3H2111 is packaged, stocked and cheap
NT3H2111, not NTAG 424 DNA	The 424 DNA would sign each tap, but has zero stock and only an NDA-drawing module package
NT3H2111, not ST25DV04KC	ST25DV is ISO 15693 (NFC-V), which phones read at shorter range
PCB coil, not a flex antenna	The card is the antenna's carrier; a coil around the edge gives the largest area and costs nothing
Programming pads on I2C	Zero cost; a fallback in case phone apps couldn't format a blank NTAG I2C plus. Not needed in the end: raw NFC commands did it (section 7)
No battery, LEDs or MCU	Keeps the card thin, wallet-safe and one part; a powered card is a different project

10. Process: how much review

Jot Rev A had two independent schematic reviews, a fault-by-fault pass and a full layout review, because it has a battery, a charger, a radio module and about 60 parts. Handshake has one part and no power source, so the review is cut to the checks that can actually fail:

Check	Jot	Handshake	Why
Architecture document	Yes	Yes	This document
Datasheet check of every pin	Yes	Yes	8 pins, checked against the datasheet at the schematic stage
Antenna calculation, two calculators	Yes	Partly	AN11276 formula and an ngspice simulation; the second calculator check was not done
Assembly check (JLCPCB)	Yes	Yes	XQFN-8 at 0.5 mm pitch; 0.8 mm board
Footprint review	Yes	Yes	Centre pad must not be soldered
Two-reviewer schematic review	Yes	No	One chip and eight pins; a datasheet pin check covers it
Power, protection, thermal	Yes	No	No power source
Measured bring-up	Yes	Partly	Read range on every Rev A card; no NanoVNA measurement

11. Close-out

One item is left to do, and only if cards are handed out: item 10. The rest are done, or closed without being done because the cards met R1 and R2 on iPhone without them.

#	Item	Status
1	Generate the coil in KiCad: `tools/make_coil.py`, 2.54 μH (5.2.1)	**Done 28 Oct**

2	Confirm L in ST eDesignSuite	Closed, not done
3	Floating SCL, SDA, VCC on a passive tag: no datasheet statement, so accepted as a risk. All five cards work with them floating	**Closed 6 Nov**
4	Footprint checked against the SOT902-3 drawing (0.5 mm pitch, no centre pad)	**Done 28 Oct**
5	JLCPCB builds 0.8 mm boards with assembly and ENIG at this quantity: five boards ordered and delivered	**Done 6 Nov**
6	Read range with the ENIG finish: about 4–5 cm	**Done 6 Nov**
7	Part, C_i, pinout and stock checked against the datasheet and JLCPCB	**Done 27 Oct**
8	Measure resonance on a NanoVNA against the 14.1 MHz prediction. Not needed to make the cards work, so the prediction is unconfirmed	Closed, not done
9	Per-card links and visit counter	Closed, not built
10	Set a write password before handing cards out (section 7)	**To do**

12. Revision history

Draft	Date	Change
1	27 October 2026	First release: block diagram, schematic, antenna calculation (4 turns, 2.56 μH), board, BOM, tag data, test plan and review scope.
2	27 October 2026	Architecture only: schematic, pin table, board sketch, layout rules and BOM removed (they belong to the schematic and layout stages); block descriptions added; R4 reworded, since the write password is a deterrent, not security.
3	28 October 2026	Coil as built (5.2.1): inset increased from 1.4 to 1.6 mm (edge to outer centreline) so the square coil corners clear the 3.18 mm board radius by 0.55 mm; L 2.54 μH, f_0 14.1 MHz. Simulation results added (5.2.2). Tuning-capacitor example updated to 2.54 μH. Pitch corrected to 0.5 mm.
3.1	28 October 2026	Status: Rev A layout complete and order files generated; tuning capacitor C1 added to the board as an unfitted 0402.
4	8 November 2026	Rev A as built: results added to the requirements and bring-up (section 8); open items closed out (section 11); blank-chip programming recorded (section 7); block diagram and web side changed to the one shared link; assembly side and artwork corrected to match the board.