Jot Rev A: Hardware Architecture

Handheld push-to-talk voice capture device with BLE sync to an iPhone app

Document	JOT-HW-001
Revision	Rev A architecture, draft 8
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Status	Schematic complete and reviewed (two independent design reviews and a fault-by-fault pass); 4-layer PCB layout complete and reviewed, including the module maker's layout review (design-rule check clean, matches the schematic); ready to order
Companion files	`BOM/Jot_RevA_BOM.xlsx` (parts, verification, design changes), `BOM/Jot_RevA_Pin_List.xlsx` (module pins, netlist), `Datasheets/`

1. Purpose

Jot is a pocketable device for capturing spoken notes. The user holds a side button, speaks, and releases. The recording is stored on the device first, then transferred to the iPhone app over Bluetooth Low Energy (BLE). The app transcribes the audio on the phone and turns it into notes, tasks, reminders, or calendar events. This document describes the Rev A custom PCB: what is on the board, how the blocks connect, and why each part was chosen.

2. Requirements

ID	Requirement	How Rev A meets it
R1	Hold to record; recording starts immediately, even from sleep	Button wakes the nRF52840 from System OFF; audio goes straight to local flash, no wait for BLE
R2	No lost recordings when the phone is out of range	32 MB flash buffer (roughly 4.5 h of Opus audio, or about 68 min of the ADPCM used on Prototype One); clips sync when the phone reconnects
R3	Recording is always visible	Rec LED is powered from the same switched rail as the microphones
R4	Feedback without looking at the device	LRA haptic motor via DRV2605L; RGB status LED; 4 kHz buzzer
R5	Days of standby; accurate battery %	TPS7A02 LDO (25 nA quiescent current), System OFF sleep, MAX17048 fuel gauge
R6	Charge and update firmware over USB-C	USB data wired to the nRF52840; UF2 bootloader for drag-and-drop updates
R7	Simple pairing	NFC tag with a flex antenna inside the back shell: tap the back of Jot to the iPhone
R8	Room to improve audio later	Footprint for a second PDM mic (not populated on Rev A)

3. Block diagram

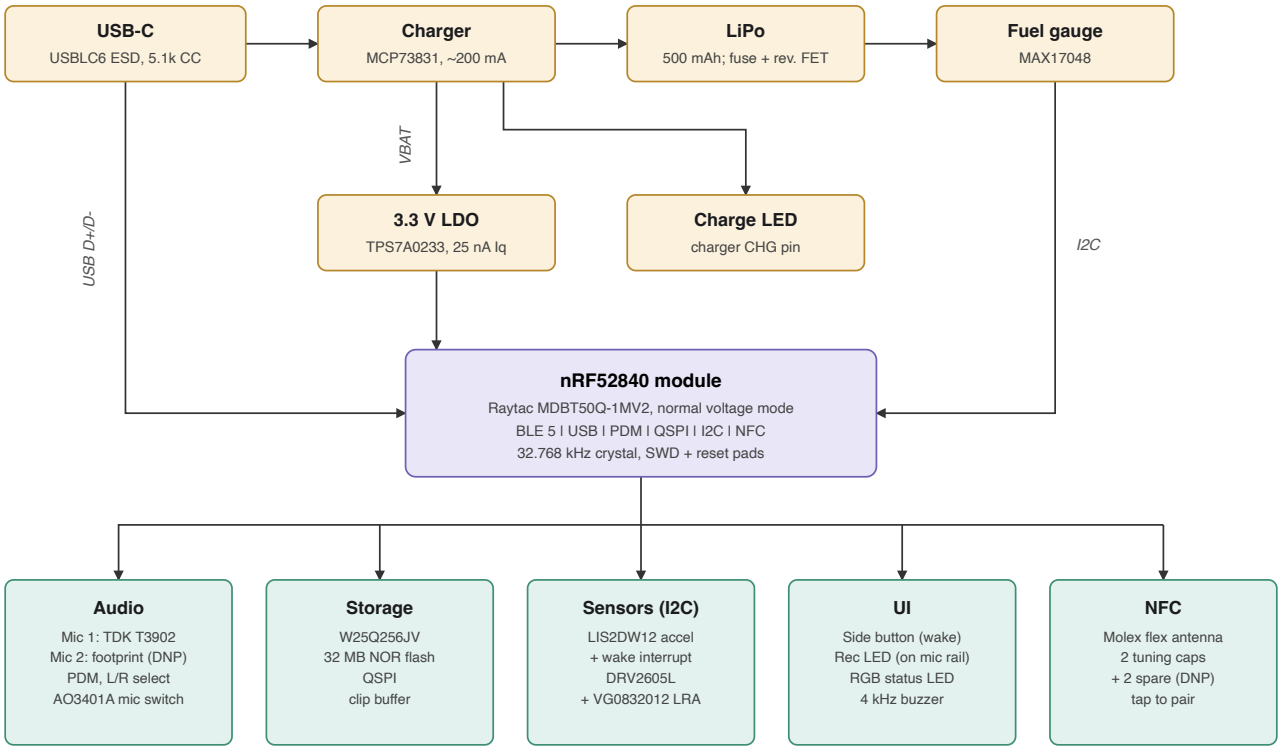


Figure 1. Rev A block diagram. Amber: power. Purple: microcontroller. Green: peripherals. The bottom groups connect to the module through the interfaces listed in Section 5.

4. Block descriptions

4.1 USB-C input

HRO TYPE-C-31-M-12 receptacle. Supplies 5 V for charging and carries USB data to the nRF52840. Two 5.1 kΩ resistors on the CC pins tell a USB-C charger to supply power; without them many chargers supply nothing. A USBLC6-2SC6 ESD protection part sits on the data lines because the connector is the part people touch. An SMF5.0A TVS diode (D5, 5 V standoff, 6.4 to 7 V breakdown) sits across VBUS next to the connector: the MCP73831 datasheet (section 6.1.1.2) requires input overvoltage protection when the supply is hot-plugged, because the cable inductance makes the voltage ring on connection. It absorbs ordinary plug-in transients; it cannot hold the module's VBUS pin (5.8 V absolute maximum) or the charger (7 V) under a large surge (see section 4.14). The module's VBUS pin is fed through a 2.2 Ω series resistor (R14), as the nRF52840 Product Specification recommends for new designs, with 10 µF to ground.

4.2 Charger

Microchip MCP73831T-2ACI/OT single-cell LiPo charger in SOT-23-5. It stops at 4.2 V. A 5.1 kΩ PROG resistor sets the charge current to about 196 mA (I_{REG} = 1000 V / R_{PROG}), which is 0.39C for the 500 mAh cell (its datasheet allows quick charge up to 1C). VDD and VBAT each have 4.7 µF, the datasheet minimum for stability when no battery is connected. The tri-state STAT pin pulls the green charge LED low while charging, so charging is visible even if the firmware is not running. The system load runs from the battery rail, as on the XIAO nRF52840.

The charger has no battery-temperature input, and the cell may only be charged between 0 and 45 °C. Rev A adds a firmware charge inhibit: the PROG resistor reaches ground through an N-MOSFET (Q7) whose gate is pulled up to VBUS by 100 kΩ (R20), so whenever USB is present the charger is enabled by default, even with the nRF52840

unpowered or in reset; a flat battery can always recover. A second N-MOSFET (Q8, gate on CHG_INHIBIT, P1.11, with a 100 kΩ pull-down R21) pulls Q7's gate low, which floats PROG and disables charging (datasheet sections 3.5 and 4.3). Firmware sets CHG_INHIBIT high outside about 5 to 40 °C, using the nRF52840 or accelerometer temperature. No 5 V reaches a GPIO. This measures board temperature, not cell temperature, and cannot act while the MCU is off (section 4.14).

Draft 3 used a TI BQ25101. Its DSBGA package has 0.4 mm ball pitch, below the 0.5 mm minimum of JLCPCB's Economic assembly (Standard assembly needs a 70 × 70 mm panel), and it cannot be reworked by hand on a first board, so it was replaced before footprints were assigned.

4.3 LiPo battery

Adafruit 1578 (PKCELL LP503035): one 3.7 V, 500 mAh lithium-polymer cell, 30 × 35 × 5.0 mm (±0.1 mm, including its protection board) by the manufacturer's drawing, with a protection circuit (Seiko S-8261 and a dual MOSFET) and a JST-PH lead with Adafruit's polarity, 100 mm long, leaving one 30 mm end. Its datasheet allows charging at 0 to 45 °C and up to 1C (500 mA), and 1C continuous discharge, against Jot's 196 mA charge and about 245 mA worst sustained load. It replaced the Adafruit 3898 (400 mAh, 36 × 17 × 7.8 mm) in draft 5 because the thinner cell takes the case from 16 mm to 12.8 mm. Adafruit's page lists 29 × 36 × 4.75 mm, so the case pocket is sized to the drawing's maximum (30.1 × 35.1 × 5.1 mm) plus swelling room. J2 is two solder holes, not a connector: the JST-PH side-entry header is 5.5 mm tall and would stand 0.8 mm into the case wall. Cut the plug off one wire at a time and solder red to J2 pad 1 (+, BATT_RAW) and black to pad 2 (–, GND); both are marked on the silkscreen. JST-PH polarity is not consistent between vendors, so check red is + with a meter before soldering.

Between J2 and the battery rail: a resettable polyfuse F1 (SMD0805P050TF: 0.5 A hold, 1 A trip; 0.33 A hold at 60 °C) and a reverse-polarity P-MOSFET Q6 (AO3401A, drain to the fuse, source to +BATT, gate to ground). The pack's own protection only trips at 2 to 5 A, so F1 covers faults between about 1 and 2 A. Worst-case sustained load is about 245 mA (radio, flash, buzzer, haptics and LEDs together) and charging is about 200 mA, both below the derated hold current. Q6 switches fully on with a correct battery (under 120 mΩ, under 30 mV at 245 mA) and stays off with a reversed one when USB is absent.

4.4 Fuel gauge (MAX17048)

Estimates battery percentage from the cell voltage using a battery model, with no current-sense resistor. It is powered from the battery, reports over I2C (address 0x36), and draws only a few microamps, so it can stay on all the time. Its open-drain ALRT output (no external pull-up: enable the nRF52840 internal pull-up) can wake the nRF52840 on low battery.

4.5 3.3 V LDO

TI TPS7A0233 (200 mA, 25 nA quiescent current, 270 mV maximum dropout at 200 mA) converts the battery voltage (about 3.0 to 4.2 V) to 3.3 V for the module, flash, accelerometer, and mic switch, with 1 μF on its input and output. Below about 3.5 V on the battery the rail follows the battery down; every 3.3 V part works down to at least 2.7 V. The nRF52840's internal high-voltage regulator (REG0) is not used: it starts at 1.8 V until firmware programs `UICR.REGOUT0`, which the 2.7 V minimum flash cannot run from, and it allows only about 25 mA for external loads, which a flash write (up to 25 mA) plus LEDs can exceed.

4.6 nRF52840 module

Raytac MDBT50Q-1MV2: a pre-certified module with chip antenna, so the RF design is already done and tested. It runs in normal voltage mode, following Raytac reference circuit 8.3: VDD and VDDH are tied to the 3.3 V rail with 10 μF, and DCCH is left unconnected, so no REG0 inductor is needed. A Seiko SC-32S 32.768 kHz crystal (12.5 pF load, the maximum the nRF52840 supports) uses two 18 pF load capacitors, from the nRF52840 PS formula (section 5.4.2.4) $C = 2 \cdot C_L - C_{pin} - C_{pcb} = 2 \times 12.5 - 4$ (typical pin capacitance) $- 3$ (estimated board stray) $= 18$ pF. The stray is an estimate; check the LFXO frequency on the built board. P0.18 is kept as a pin reset on a test pad, alongside the SWD pads. The antenna end of the module goes at the board edge with no copper underneath, and away from the battery and the user's hand.

4.7 Audio

Mic 1 is a TDK T3902 bottom-port PDM MEMS microphone (64 dBA SNR, 1.65 to 3.63 V). It replaced the planned Infineon IM69D130 (69 dB SNR) because the T3902 is stocked at LCSC. Bottom port means the sound enters through a hole in the PCB under the mic; this fixes which board face points at the case opening. Mic 1's SELECT pin is grounded (right channel). A footprint for Mic 2 shares the same two PDM wires with SELECT tied high (left channel) and is not populated on Rev A (DNP). Both mics and the Rec LED are powered from a switched rail: an AO3401A P-MOSFET with a 100 kΩ gate pull-up, so the rail is off by default and on when the GPIO drives low. Firmware should release the PDM clock pin while the rail is off.

4.8 Storage

Winbond W25Q256JVEIQ: 256 Mbit (32 MB) NOR flash on QSPI, WSON-8 8 × 6 mm, quad mode fixed on at the factory (QE = 1 for the IQ option). It replaced the 128 MB W25Q01JV in draft 5: same package and pinout, $4.34 instead of $36.51 per board, and 32 MB is about 68 minutes of 8 KB/s audio, ample between syncs. It powers up in 3-byte addressing; firmware switches to 4-byte mode (instruction B7h) to reach above 16 MB. Its read voltage must stay within ±10% of the voltage the data was written at, so firmware blocks writes below the low-battery cutoff. A 100 kΩ pull-up holds chip-select high while the nRF52840 powers up or resets, as Winbond requires. Recordings are written here first and deleted once the phone confirms it has them.

4.9 Sensors on I2C

LIS2DW12 low-power accelerometer (address 0x19, SA0 tied high: its internal pull-up cannot be switched off, so tying it low would draw about 150 μA): detects raise-to-wake, double-tap, and shake in hardware and signals the nRF52840 on an interrupt pin, so the main chip can stay asleep. DRV2605L haptic driver (address 0x5A), powered from the battery with 1 μF on VDD and on REG, drives a Vybronics VG0832012 LRA (8 mm coin, 235 Hz, 1.8 Vrms) for crisp taps from a built-in effect library. Both share the I2C bus with the fuel gauge; one pair of 2.2 kΩ pull-ups serves the whole bus. They were 4.7 kΩ until draft 5: the MAX17048 alone may add 60 pF and requires a 300 ns maximum rise time, which left only about 15 pF of margin ($t_r \approx 0.85 \cdot R \cdot C$); 2.2 kΩ allows about 160 pF. The extra current (1.5 mA per line) flows only during transfers.

4.10 UI

Side button: TS-1010-C-A right-angle tactile switch to ground through a 1 kΩ series resistor (R5, placed at the module) that limits ESD current into the pin, using the internal pull-up; it is also the wake source. Rec LED: red 0603 on the mic rail through 1 kΩ. RGB status LED: common-anode 1615 RGB with the anode on the battery rail. Each cathode is switched to ground by an AO3400A (gate from a PWM pin, 100 kΩ pull-down) through 1 kΩ (red) and 560 Ω (green, blue), about 2 mA at 3.7 V. Green and blue need about 2.6 V at 2 mA (up to about 3.0 V worst case), and the 3.3 V rail falls to about 3.0 V as the battery empties, so driving them from a 3.3 V pin left no headroom whatever the resistor. From the battery they keep more headroom: at the 3.3 V firmware cutoff green and blue still get about 0.5 mA (dim but lit); a 3.0 V cell leaves no guaranteed margin, so use red for the low-battery warning. No GPIO sees the battery voltage. Draft 2 drove a common-cathode TJ-S1615 from GPIOs through 100 Ω, which does not fix the headroom. Buzzer: MLT-5020 magnetic buzzer, 4 kHz, from the battery rail through a 10 Ω, 1 W series resistor in a 2512 package (R19; the buzzer is rated 2 to 4 V and the battery reaches 4.2 V; if Q1 were left on, R19 would dissipate about 0.49 W) and an AO3400A low-side MOSFET, with a 1N4148W flyback diode across the buzzer, for confirmation tones and a find-my-Jot feature.

4.11 NFC

The nRF52840 has an NFC tag built in. Rev A uses an off-the-shelf flexible antenna, the Molex 146236-0101 (15 × 25 mm plus a solder-pad tab, 0.27 mm thick, 3.1 μH, Q 51.8, with a ferrite layer), stuck into a 0.35 mm pocket in the back shell's floor with the ferrite towards the battery. Two fine wires run from its tab, past the top end of the battery, to AE1: two solder-wire holes at the right edge of the PCB, about 12 mm from the Bluetooth antenna. Two equal C0G tuning capacitors (C16, C17) from NFC1 and NFC2 to ground form an LC tank at 13.56 MHz. Tapping the back of Jot to the iPhone can open the app or start pairing.

A coil drawn on the PCB was the plan until layout. It needs about 20 × 20 mm with no copper on any layer inside it, and the only metal-free part of the board is the Bluetooth antenna corner; everywhere else the battery sits behind the board.

The ferrite-backed flex antenna takes no board area and works over the battery, the way a phone's NFC antenna does.

$$C_{tune} = 2 / ((2\pi \cdot 13.56\ \text{MHz})^2 \cdot L_{ant}) - C_p - C_{int}, \quad C_{int} \approx 4\ \text{pF}$$

From the nRF52840 Product Specification (v1.11, section 6.14.10, page 461) and Nordic white paper nWP-026 (in `Datasheets/NFC/`), with L_{ant} = 3.1 μH and $C_p \approx 2$ pF: 88.9 – 2 – 4 = 82.9 pF, so C16 and C17 are 82 pF (C0G, 0402). The datasheet inductance is measured in free space; the battery behind the ferrite will shift it. C18 and C19 are empty 0402 pads in parallel with C16 and C17 for tuning on the first built board: measure the resonance (S11 dip) with a network analyzer or a phone read-range test, then add equal capacitance to both sides if the resonance is above 13.56 MHz, or swap C16/C17 for a lower value if it is below ($f = 1 / (2\pi\sqrt{LC})$). Keep both sides equal and the two tracks mirrored.

4.12 Power budget (estimate)

First-pass estimates from the component datasheets (typical values at 25 °C), to be replaced by measurements at bring-up.

Mode	Current (typ)	Main contributors
Standby (System OFF)	≈10 to 17 μA	DRV2605L shutdown 4 μA, MAX17048 hibernate 3 μA, cell protection ≤7 μA (max), flash deep power-down 1 μA, LIS2DW12 low-power 1 μA, nRF52840 System OFF 0.4 μA
Recording (Opus, DC/DC on)	≈6.2 mA (≈9.2 mA with DC/DC off)	CPU 3.3 mA, Rec LED ≈1.3 mA, flash program and erase ≈0.6 mA, PDM ≈0.5 mA (assumed), mic 0.43 mA
BLE sync	≈8 mA for about 1 min a day	Radio TX at 0 dBm 6.4 mA, RX 6.3 mA

With 400 mAh usable (80% of 500 mAh), the electronics alone allow over two years of standby, so the cell's own self-discharge sets the real limit and R5 is met with a wide margin. A typical day (ten one-minute recordings and one sync) uses about 1.6 mAh, roughly 250 days per charge (about 190 days with the DC/DC regulator off). Firmware must put the flash into deep power-down before System OFF (its standby current is 10 μA typical, 60 μA maximum, against 1 μA in power-down; W25Q256JV datasheet, ICC1 and ICC2), enable the DC/DC regulator, and keep the haptic driver's EN pin low.

4.13 Bring-up and test plan

Check the battery lead polarity, then feed the battery input from a bench supply at 3.7 V with a 50 mA current limit. Confirm the 3.3 V rail, that idle current is in the microamp range, and that nothing runs warm. Then, in order: probe the LDO output and the module's VDD; flash a blinky over SWD and check reset; scope the 32.768 kHz crystal once firmware starts it; read the flash JEDEC ID over QSPI, then write and read back across both dies; find the three I2C parts (0x19, 0x36, 0x5A); switch on the mic rail, confirm the Rec LED, and capture and play back PDM audio; pair over BLE and transfer a clip; test USB charging and the UF2 bootloader; check that CHG_INHIBIT stops and restarts charging; scope VBUS at the charger and at the module when plugging in a cable (hot-plug overshoot against 7 V and 5.8 V); with USB unplugged, confirm a reversed battery draws no current. Finally, measure every mode on the battery input with a power profiler (Nordic PPK2) and update section 4.12 with real numbers.

4.14 Protection summary and known Rev A limitations

Draft 5 came from a fault-by-fault design review: for every rail, what limits the current if something shorts, and what each part sees in a single fault. The 3.3 V rail is limited by the LDO's foldback current limit; the battery rail by F1 and the pack's protection; the USB input by the source. Rev A is a development build; these limits are accepted and documented, each with a test at bring-up and a Rev B fix:

Limitation	Why it is accepted on Rev A	Rev B fix

Reversed battery while USB is connected: the charger drives +BATT, which turns Q6 on, and a few tens of mA can flow into the reversed cell	Battery wires soldered and polarity-checked with a meter by the builder; the common case (reversed pack, no USB) is blocked	Reverse-polarity switch that stays off with either USB state (Analog Devices AN-171 approach) or an ideal-diode controller
Charge temperature: firmware inhibit uses board temperature and cannot act while the MCU is off	Development units charged indoors at room temperature; the inhibit covers the normal case	Charger with an NTC input and a thermistor on the cell
VBUS surge: D5 clamps ordinary hot-plug transients but not every surge below the module's 5.8 V and the charger's 7 V absolute maximum	Matches common practice for small USB devices; overshoot is measured at bring-up	Overvoltage-protection load switch on VBUS
A short at the buzzer (for example a solder bridge) puts about 1.8 W into R19, below F1's hold current	A manufacturing fault: inspected at assembly; R19 kept away from the cell	Current-limited buzzer drive
VBUS capacitance 14.7 μF (C1 + C7) is above the USB 10 μF guideline	Chargers and phones tolerate it	Reduce C7 or add soft-start

Firmware rules the hardware relies on: drive the buzzer only from the PWM peripheral; low-battery cutoff at about 3.3 to 3.4 V (the pack only cuts off at 2.5 V) and no flash writes below it; FG_ALRT internal pull-up; CHG_INHIBIT high outside about 5 to 40 °C while USB is present; release the PDM pins before switching the mic rail off; flash 4-byte addressing; I2C at 100 kHz.

5. Interfaces

Each connection in Figure 1 uses a standard interface. Knowing these makes the schematic much easier to read. The exact pin for each signal is in the pin list.

Interface	Wires	Used for	What to know
I2C	2 (SDA, SCL) + pull-up resistors	Fuel gauge, accelerometer, haptic driver	Shared bus; each chip has its own address (0x36, 0x19, 0x5A, no conflicts). Needs one pair of pull-ups on the whole bus (2.2 kΩ), not one per chip.
PDM	2 (clock, data)	Microphones	Digital audio from the mic. Two mics can share the wires, one on each clock edge (left/right).
QSPI	6 (clock, chip select, 4 data)	32 MB flash	SPI with four data lines for speed. The nRF52840 selects QSPI pins in firmware; Rev A uses the nRF52840 DK's set (CSN P0.17, SCK P0.19, IO0 to IO3 on P0.20 to P0.23) with high-drive outputs. The PS lists P0.18/P1.00 as an alternative, but P0.18 is the reset pin.
USB	2 (D+, D-)	Firmware updates, debug	Full-speed USB is built into the nRF52840; no extra USB chip needed.
SWD	2 (SWDIO, SWCLK) + GND, 3.3 V, reset	Programming and debugging	Used with a debug probe for the first flash and for step-through debugging.

NFC	2 (NFC1, NFC2)	Flex antenna (AE1)	Dedicated pins on the nRF52840; the antenna and caps form a tuned circuit at 13.56 MHz.
GPIO / PWM	1 per signal	Button, LEDs, buzzer, mic power switch, interrupts	Plain digital pins. PWM sets LED brightness and buzzer tone. Pins near the radio are low-frequency only and carry only slow signals.

6. Key design decisions

Decision	Choice	Reason
Wireless link	BLE only, store-and-forward	Low power; recording never waits for a connection
Radio implementation	Pre-certified module, not a bare chip	Avoids RF layout risk on a first board
3.3 V supply	External TPS7A02 LDO; nRF in normal voltage mode	Correct voltage from first power-up and no 25 mA external-load limit, at 25 nA standby cost
Microphone	TDK T3902	In stock at LCSC; 64 dBA SNR. The IM69D130 (69 dB) was the first choice
Storage size	32 MB flash, not microSD	Clips only live on the device until synced; flash is smaller, lower power, no moving parts. 32 MB (about 68 min of audio) instead of 128 MB saves about $32 a board
Battery protection	Polyfuse + reverse-polarity P-FET; firmware charge inhibit	Covers faults below the pack's 2 A trip, a reversed pack, and charging outside 0 to 45 °C, for units given to other people
Recording indicator	LED on the mic power rail	Recording cannot happen without the light being on
Haptics	DRV2605L + LRA	Crisp, phone-like feedback; effect library saves firmware work
Flash pins	nRF52840 DK QSPI pin set	Keeps P0.18 as a working pin reset; matches the DK's Zephyr board files
Second mic	Footprint only (DNP)	Keeps Rev A simple while leaving room for noise reduction later
Deferred to Rev B	Charging dock, wireless charging, display	Limits risk on the first spin

7. Open items

#	Item	Status	Outcome
1	Confirm the mic port type and LCSC stock	**Done**	TDK T3902 (bottom port, LCSC C3171752)
2	Pick the module and confirm it exposes the QSPI, USB, and NFC pins	**Done**	Raytac MDBT50Q-1MV2; all pins confirmed against its datasheet. Pre-ordered through JLCPCB (C5118826) on 8 October, with the DRV2605L (low stock)
3	Pick the flash part and confirm the Zephyr driver supports its 4-byte addressing	**Part done**	W25Q256JVEIQ (32 MB) chosen in draft 5. Confirm Zephyr 4-byte addressing during firmware bring-up
4	Select charger and LDO from in-stock LCSC parts	**Done**	MCP73831T-2ACI/OT (C424093), TPS7A0233 (C2887324). The BQ25101 was dropped in draft 4: its 0.4 mm BGA is below JLCPCB Economic assembly limits.

5	Choose the LRA size to fit the case	**Part done**	Vybronics VG0832012 (8 mm); confirm fit in the case
6	Battery capacity and dimensions (set by the case)	**Done**	Adafruit 1578 (PKCELL LP503035), 500 mAh, 30 × 35 × 5.0 mm; fits the 12.8 mm case; check its polarity with a meter before first plug-in
7	Assign every signal to a module pin (pin map)	**Done**	See `BOM/Jot_RevA_Pin_List.xlsx`
8	NFC antenna and tuning capacitor values	**Part done**	Molex 146236-0101 chosen, C16/C17 82 pF calculated (section 4.11). Tune on the first built board with C18/C19
9	Pick an in-stock common-anode 1615 RGB LED for the battery-rail drive (section 4.10)	**Done**	TOGIALED TJ-S1615SW6TGLCCYRGB-A5 (LCSC C273610), same family and pads as the common-cathode part it replaces: pin 1 anode, 2 blue, 3 green, 4 red. Q3-Q5 AO3400A with R15-R17 100k pull-downs; R8 1k, R9/R10 560 Ω. BOM and pin list updated 4 October.
10	Give the mic its own T3902 symbol	**Done**	Jot:T3902 symbol with the TDK datasheet and MPN; it keeps KiCad's Knowles LGA-5 footprint, whose pins, pads and port were checked against the T3902 datasheet and match. Netlist unchanged
11	Raytac antenna and layout review	**Part done**	Reviewed 29 October; layout updated 4 November: 3.8 mm keep-out across the full board width on all layers, ground poured on both outer layers and stitched to layer 2 (158 ground vias), ground under the module on layer 3, crystal load capacitors symmetric with ground around them, 10 mil module supply tracks. Final check with Raytac before ordering.
12	Rev B protection items (section 4.14)	**Open**	Reverse switch with USB, NTC charger, VBUS overvoltage switch, current-limited buzzer

8. Revision history

Draft	Date	Changes
1	October 2026	First architecture.
2	2 October 2026	Parts selected and checked against datasheets; mic changed to TDK T3902; external LDO confirmed (REG0 unused); R14 and 10 μF decoupling added; QSPI pin note corrected; NFC tuning method added.
3	3 October 2026	Crystal load-cap calculation written out with board stray; RGB LED moved to the battery rail with low-side FETs; mic footprint checked against the T3902 datasheet; power budget and bring-up plan added. 4 October: accelerometer address changed to 0x19 (SA0 high) to avoid current through its internal pull-up.
4	5 October 2026	Charger changed from TI BQ25101 (0.4 mm-pitch DSBGA, not assemblable by JLCPCB Economic PCBA) to Microchip MCP73831 in SOT-23-5 with a 5.1 kΩ PROG resistor and 4.7 μF on VDD and VBAT. Schematic review (4 October) added a 100 kΩ pull-up on the flash chip-select and a 10 Ω resistor in series with the buzzer.

5	8 October 2026	After a fault-by-fault design review: polyfuse F1 and reverse-polarity P-FET Q6 at the battery connector; SMF5.0A TVS on VBUS; firmware charge inhibit (Q7, Q8, R20, R21, CHG_INHIBIT on P1.11); buzzer resistor R19 to 1 W 2512; I2C pull-ups 4.7 kΩ to 2.2 kΩ; 1 kΩ series resistor on the button; flash changed to the 32 MB W25Q256JV; NFC tuning direction corrected; LED low-battery claim corrected; protection summary and known limitations added (section 4.14). Battery changed to the Adafruit 1578 (500 mAh, 5.0 mm thick) for a 12.8 mm case.
6	14 October 2026	NFC antenna changed from a PCB coil to a Molex 146236-0101 ferrite-backed flex antenna in the back shell, found at layout to be the only way to fit NFC beside the battery and the Bluetooth antenna. AE1 became two solder-wire holes; C16/C17 recalculated to 82 pF; C18/C19 added as unpopulated tuning pads (section 4.11).
7	16 October 2026	PCB layout complete after a full layout review. J2 changed from a JST-PH header to two solder-wire holes: the side-entry header is 5.5 mm tall and would not fit the 12.8 mm case. LED drive pins re-assigned to match the transistor order on the board: P1.08 red, P0.11 green, P0.12 blue. No via drilled inside an SMD pad; no top-layer signals or vias beside the crystal; buzzer resistor R19 moved off the battery; extra ground vias at the module and decoupling capacitors.
8	4 November 2026	Layout updated after Raytac's antenna and layout review: 3.8 mm keep-out across the full board width on all layers; ground poured on the top and bottom layers and stitched to the layer 2 ground plane (158 ground vias); layer 3 under the module changed from 3.3 V to ground, with 3.3 V routed around it; crystal load capacitors C8/C9 placed symmetrically and turned the same way, with ground poured around the crystal traces; VDD, VDDH and the module's VBUS tracks widened to 10 mil. No schematic change.